Electronic Devices (Semiconductor Devices)

Short notes for B.Tech ECE · EEE · GATE EC

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I. Semiconductor Basics

- **Energy bands**: valence band (bound electrons), conduction band (free electrons), and the forbidden gap Eg between them.
- Insulator: Eg large (> 5 eV). Semiconductor: Eg about 1 eV. Conductor: bands overlap.

Material	Eg at 300 K	Type of band gap
Silicon (Si)	1.12 eV	Indirect
Germanium (Ge)	0.66 eV	Indirect
Gallium arsenide (GaAs)	1.42 eV	Direct (good for LEDs, lasers)

- **Intrinsic** semiconductor: pure, n = p = ni. For Si at 300 K, ni ≈ 1.5 x 10^10 cm^-3 (some books use 10^10).
- **Extrinsic**: doped. **n-type** = donor (group V: P, As, Sb). **p-type** = acceptor (group III: B, Al, Ga, In).
- Eg falls slightly as temperature rises. ni rises very fast with temperature.

FORMULA Mass action law: n x p = ni^2 (in thermal equilibrium, for both intrinsic and extrinsic).

FORMULA ni^2 is proportional to T^3 e^(−Eg / kT).

➤ Fermi level

- **Fermi level EF**: energy where the probability of occupation is 1/2. Fermi–Dirac: f(E) = 1 / (1 + e^((E − EF)/kT)).
- Intrinsic: EF near the middle of the gap. n-type: EF moves towards Ec. p-type: EF moves towards Ev.

- $n = n_i e^{((E_F - E_i)/kT)}$, $p = n_i e^{((E_i - E_F)/kT)}$.

2. Carrier Transport

- **Drift**: motion due to electric field. Drift velocity $v = \mu E$ (μ = mobility).
- **Diffusion**: motion from high concentration to low concentration. $J_{n(diff)} = q D_n dn/dx$, $J_{p(diff)} = -q D_p dp/dx$.
- Mobility of electrons > holes (Si: $\mu_n \approx 1350$, $\mu_p \approx 480$ cm^2/V·s). Mobility falls with higher doping and higher temperature.

FORMULA Conductivity $\sigma = q(n \mu_n + p \mu_p)$. Resistivity $\rho = 1 / \sigma$.

FORMULA Einstein relation: $D_n / \mu_n = D_p / \mu_p = V_T = kT / q \approx 0.0259$ V at 300 K.

➤ Solved example (n-type silicon)

- Si doped with $N_D = 10^{16}$ cm^-3, $\mu_n = 1350$ cm^2/V·s, $n_i = 1.5 \times 10^{10}$ cm^-3.
  - $n \approx N_D = 10^{16}$ cm^-3
  - $p = n_i^2 / n = (2.25 \times 10^{20}) / 10^{16} =$ 2.25 x 10^4 cm^-3 (minority holes)
  - $\sigma \approx q n \mu_n = 1.6 \times 10^{-19} \times 10^{16} \times 1350 =$ 2.16 S/cm
  - $\rho = 1 / 2.16 = 0.463\ \Omega\cdot$cm

➤ Hall effect

- Current in x, magnetic field B in z → Hall voltage in y. Sign of V_H tells whether the sample is n-type or p-type.

FORMULA Hall coefficient $R_H = 1 / (q n)$ (magnitude). $V_H = B I / (q n w)$, where w = thickness along B. Mobility $\mu = \sigma R_H$.

➤ Generation, recombination, continuity

- **Lifetime τ**: average time before an excess carrier recombines. Diffusion length $L = \sqrt{D \tau}$.
- Continuity equation (holes in n-type): $\partial p/\partial t = -(p - p_0)/\tau_p - (1/q) \partial J_p/\partial x + G_p$.
- In Si (indirect gap), recombination happens mainly through traps (SRH recombination).

3. PN Junction Diode

- At the junction, carriers diffuse and leave behind fixed ions → **depletion region** with a built-in field.

FORMULA Built-in potential $V_0 = V_T \ln(N_A N_D / n_i^2)$.

FORMULA Depletion width $W = \sqrt{(2\varepsilon(V_0 - V)/q) \times (1/N_A + 1/N_D)}$. It extends more into the lightly doped side.

➤ Solved example (built-in potential)

- $N_A = 10^{17}\ cm^{-3}$, $N_D = 10^{16}\ cm^{-3}$, $n_i = 1.5 \times 10^{10}\ cm^{-3}$, $V_T = 0.0259$ V.
  - $N_A N_D / n_i^2 = 10^{33} / 2.25 \times 10^{20} = 4.44 \times 10^{12}$
  - $\ln(4.44 \times 10^{12}) = 1.49 + 27.63 = 29.12$
  - $V_0 = 0.0259 \times 29.12 =$ **0.754 V**

➤ Diode equation

FORMULA $I = I_0 (e^{V/\eta V_T} - 1)$. $\eta = 1$ for Ge, about 1 to 2 for Si.

- I_0 (reverse saturation current) doubles for every 10 °C rise.
- Cut-in voltage: Si ≈ 0.7 V, Ge ≈ 0.3 V. Forward voltage falls about 2.5 mV per °C.
- Dynamic resistance $r_d = \eta V_T / I$ (about 26 Ω at 1 mA with $\eta = 1$).

➤ Junction capacitances

Capacitance	Bias	Cause	Formula
Transition (depletion) C_T	Reverse	Change of depletion charge	$C_T = \varepsilon A / W$, $C_T \propto (V_0 + V_R)^{(-1/2)}$ for abrupt junction
Diffusion C_D	Forward	Stored minority charge	$C_D = \tau I / (\eta V_T)$

➤ Breakdown

Point	Zener breakdown	Avalanche breakdown
Doping	Heavy	Light
Breakdown voltage	Low (< about 5 V)	High (> about 7 V)
Mechanism	Field pulls electrons out of bonds (tunnelling)	Impact ionisation, carrier multiplication
Temperature coefficient	Negative	Positive

4. Special Diodes

Device	Key idea	Use
Zener diode	Works in reverse breakdown	Voltage regulator, reference
LED	Forward bias, recombination emits light (direct gap)	Indicators, displays
Photodiode	Reverse bias, light makes current	Light sensor, optical receiver
Solar cell	No bias, light makes power	Energy conversion
Varactor	Reverse bias, CT changes with voltage	Tuning, VCO
Tunnel diode	Very heavy doping, negative resistance region	Microwave oscillator
Schottky diode	Metal–semiconductor, majority carriers only	Fast switching, low drop (≈ 0.3 V)
PIN diode	Intrinsic layer between p and n	RF switch, photodetector

FORMULA LED wavelength λ (μm) ≈ 1.24 / Eg (eV). For GaAs, $\lambda \approx 1.24 / 1.42 = 0.87$ μm (infrared).

5. Bipolar Junction Transistor (BJT)

- Three regions: emitter (heavily doped), base (thin, lightly doped), collector (moderately doped, largest).

FORMULA $I_E = I_B + I_C$, $\alpha = I_C / I_E$, $\beta = I_C / I_B$, $\beta = \alpha / (1 - \alpha)$, $\alpha = \beta / (1 + \beta)$.

EXAMPLE $\alpha = 0.98 \rightarrow \beta = 0.98 / 0.02 = 49$.

Modes of operation

Mode	E–B junction	C–B junction	Use
Active	Forward	Reverse	Amplifier
Saturation	Forward	Forward	Closed switch
Cut-off	Reverse	Reverse	Open switch
Reverse active	Reverse	Forward	Rarely used

- **Early effect** (base-width modulation): higher VCB → wider C–B depletion → narrower effective base → IC rises slightly with VCE. Gives finite output resistance $r_o = V_A / I_C$.
- **Punch-through**: the C–B depletion region reaches the emitter at very high VCB.
- Ebers–Moll model describes the BJT in all modes.

6. Field-Effect Transistors

JFET

- Voltage-controlled, unipolar (only majority carriers), very high input resistance.

FORMULA Shockley equation: $I_D = I_{DSS} (1 - V_{GS} / V_P)^2$ for $V_P \le V_{GS} \le 0$ (n-channel).

MOSFET

- Metal–oxide–semiconductor structure. Input current ≈ 0 (insulated gate).
- **Enhancement** type: no channel at $V_{GS} = 0$, needs $V_{GS} > V_T$. **Depletion** type: channel exists at $V_{GS} = 0$.

Region	Condition (NMOS)	Drain current
Cut-off	$V_{GS} < V_T$	$I_D = 0$
Linear (triode)	$V_{GS} > V_T$, $V_{DS} < V_{GS} - V_T$	$I_D = \mu_n C_{ox} (W/L) [(V_{GS} - V_T) V_{DS} - V_{DS}^2 / 2]$
Saturation	$V_{GS} > V_T$, $V_{DS} \ge V_{GS} - V_T$	$I_D = (1/2) \mu_n C_{ox} (W/L) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

➤ Solved example (MOSFET in saturation)

- μn Cox = 200 μA/V^2, W/L = 10, VT = 0.5 V, VGS = 1.5 V, VDS = 2 V, λ = 0.
  - VGS − VT = 1 V and VDS = 2 V > 1 V → saturation
  - ID = 0.5 x 200 μA x 10 x (1)^2 = 1 mA
  - gm = 2 ID / (VGS − VT) = 2 x 1 mA / 1 V = 2 mA/V

➤ MOS capacitor and threshold

- As VG rises (p-substrate): accumulation → depletion → inversion. VT is the gate voltage that starts strong inversion.
- VT rises with substrate doping and with thicker oxide. **Body effect**: VT rises when the source–body voltage rises.
- Cox = εox / tox (per unit area).
- **Short-channel effects**: channel length modulation, DIBL, velocity saturation, hot carriers.

➤ BJT vs MOSFET

Point	BJT	MOSFET
Control	Current controlled	Voltage controlled
Carriers	Both (bipolar)	Majority only (unipolar)
Input impedance	Low to medium	Very high
Transconductance	Higher (IC / VT)	Lower
Use	Analog, high gain	Digital ICs, low power (CMOS)

7. IC Fabrication (basics)

1. **Crystal growth** (Czochralski) and wafer preparation.
2. **Oxidation**: grow SiO2 (dry oxide = better quality, wet oxide = faster).
3. **Photolithography**: photoresist, mask, expose, develop, etch.
4. **Diffusion** and **ion implantation**: add dopants (implantation gives better control).
5. **Deposition** (CVD) of polysilicon, nitride, oxide; **metallisation** (Al or Cu).
6. **Etching**: wet (isotropic) or dry/plasma (anisotropic).

> **REMEMBER** In a CMOS n-well process, the NMOS is made in the p-substrate and the PMOS in the n-well.

8. Most Asked Questions (practice)

1. Explain energy band diagrams of intrinsic, n-type and p-type semiconductors.
2. State the mass action law and find minority carrier concentration.
3. Derive the Einstein relation. Find conductivity of a doped sample.
4. Explain the Hall effect and how it finds carrier type and concentration.
5. Derive the built-in potential and depletion width of a PN junction.
6. Compare Zener and avalanche breakdown. Compare transition and diffusion capacitance.
7. Explain the working of LED, photodiode, solar cell and tunnel diode.
8. Derive $\beta = \alpha / (1 - \alpha)$. Explain the Early effect.
9. Explain MOSFET operation in all regions and find ID in saturation.
10. List the main steps of CMOS fabrication.

TIP GATE EC devices questions are mostly numericals: carrier concentration, conductivity, built-in potential, depletion width and MOSFET current. Keep q, kT/q and n_i values ready.