Microprocessors and Microcontrollers (8085, 8086, 8051)

Short notes for B.Tech ECE · EEE · CSE · GATE EC

Uncodemy Handwritten Notes · free for students

1. Introduction

- **Microprocessor** = CPU on a single chip (ALU + registers + control unit). Needs external memory and I/O.
- **Microcontroller** = CPU + RAM + ROM + I/O ports + timers + serial port on one chip (a small computer).
- **Bus**: address bus (one way, selects location), data bus (two way), control bus (RD, WR, etc.).

Point	Microprocessor	Microcontroller
Memory, I/O	External	On-chip
Cost, size	Higher, bigger system	Lower, compact
Use	General computing	Embedded control (washing machine, remote)
Example	8085, 8086	8051, PIC, AVR

- **Von Neumann**: one memory and bus for program and data. **Harvard**: separate program and data memories (8051 follows Harvard).

2. 8085 Architecture

- 8-bit microprocessor, 40 pins, +5 V supply, 16-bit address bus → 64 KB memory.
- Lower address and data are multiplexed: **AD0–AD7**. **ALE** (address latch enable) separates them with a latch.
- Clock: crystal frequency is divided by 2 internally (6 MHz crystal → 3 MHz operation).

Registers

- Accumulator **A** (8-bit), general purpose **B**, **C**, **D**, **E**, **H**, **L** (pairs BC, DE, HL for 16-bit use).
- **PC** (program counter, 16-bit): address of the next instruction. **SP** (stack pointer, 16-bit): top of stack.
- **Flag register**: 5 flags.

Flag	Set when
S (sign)	D7 of the result = 1
Z (zero)	Result = 0
AC (auxiliary carry)	Carry from D3 to D4 (used for BCD, DAA)
P (parity)	Result has even number of 1s
CY (carry)	Carry or borrow out of D7

Interrupts of 8085

Interrupt	Vector address	Type	Maskable?
TRAP (RST 4.5)	0024H	Edge and level	No (highest priority)
RST 7.5	003CH	Rising edge	Yes
RST 6.5	0034H	Level	Yes
RST 5.5	002CH	Level	Yes
INTR	From external device (RST n)	Level	Yes (lowest priority)

FORMULA Vector of RST n = n x 8 (in hex). Example: RST 5.5 → 5.5 x 8 = 44 = 002CH.

- SIM sets interrupt masks and serial output (SOD). RIM reads masks, pending interrupts and serial input (SID).

Machine cycles and timing

- **T-state** = one clock period. **Machine cycle** = one bus operation (opcode fetch, memory read/write, I/O read/write).
- Opcode fetch = 4 T (6 T for some instructions like DCX, INX, PCHL). Memory read = 3 T.
- Example: `MVI A, 32H` = opcode fetch (4 T) + memory read (3 T) = 7 T. `LDA 2050H` = 4 + 3 + 3 + 3 = 13 T.

3. 8085 Instruction Set and Programming

Group	Examples
Data transfer	MOV, MVI, LDA, STA, LXI, LHLD, SHLD, XCHG
Arithmetic	ADD, ADI, ADC, SUB, INR, DCR, INX, DAD, DAA
Logical	ANA, ORA, XRA, CMP, RLC, RRC, RAL, RAR, CMA
Branch	JMP, JZ, JNZ, JC, CALL, RET, RST
Machine control	HLT, NOP, EI, DI, SIM, RIM, PUSH, POP

➤ Addressing modes

Mode	Example	Meaning
Immediate	MVI B, 45H	Data is in the instruction
Register	MOV A, B	Data in a register
Direct	LDA 2000H	Address is in the instruction
Register indirect	MOV A, M	Address is in HL pair
Implied	CMA	Operand is implied (accumulator)

➤ Example program: add two 8-bit numbers

```
LDA 2050H   ; A = first number
MOV B, A    ; B = first number
LDA 2051H   ; A = second number
ADD B       ; A = A + B
STA 2052H   ; store sum
HLT
```

➤ Solved example (delay loop)

```
      MVI C, FFH   ; 7 T
LOOP: DCR C        ; 4 T
      JNZ LOOP     ; 10 T if jump, 7 T if not
```

- FFH = 255 counts.
  - DCR runs 255 times = 255 x 4 = 1020 T
  - JNZ jumps 254 times (10 T) and falls through once (7 T) = 2540 + 7 = 2547 T
  - Total = 7 + 1020 + 2547 = **3574 T-states**
  - With a 3 MHz clock (T = 0.333 µs): delay = 3574 / 3 x 10^6 = **1.19 ms**

4. 8086 Architecture

- 16-bit microprocessor, 20-bit address bus → 1 MB memory, 16-bit data bus, 40 pins.
- Divided into **BIU** (bus interface unit) and **EU** (execution unit). They work in parallel = **pipelining**.
- BIU has a 6-byte instruction queue (pre-fetch), segment registers and IP. EU has ALU, general registers and flags.

➤ Registers

- General: AX, BX, CX, DX (each splits into high/low bytes, e.g. AH, AL).
- Pointer and index: SP, BP, SI, DI. Segment: **CS** (code), **DS** (data), **SS** (stack), **ES** (extra). IP = instruction pointer.
- **Flags** (9): 6 status (CF, PF, AF, ZF, SF, OF) + 3 control (TF = trap/single step, IF = interrupt enable, DF = direction for strings).

FORMULA Physical address = segment x 10H + offset (shift segment left by 4 bits and add).

EXAMPLE CS = 2000H, IP = 1234H. Physical address = 20000H + 1234H = 21234H.

- Each segment can be up to 64 KB. Segments can overlap.

➤ Modes and other points

- **Minimum mode** (MN/MX = 1): single processor, 8086 makes the control signals.
- **Maximum mode** (MN/MX = 0): multiprocessor system, 8288 bus controller makes control signals.
- **Interrupt vector table**: 00000H to 003FFH, 256 interrupts x 4 bytes (CS and IP). Address of type n = 4 x n.
- Type 0 = divide error, type 1 = single step, type 2 = NMI, type 3 = breakpoint, type 4 = overflow.
- Addressing modes: immediate, register, direct, register indirect, based, indexed, based-indexed, relative.

➤ 8085 vs 8086

Point	8085	8086
Data bus	8-bit	16-bit
Address bus	16-bit (64 KB)	20-bit (1 MB)
Pipelining	No	Yes (6-byte queue)
Memory segmentation	No	Yes
Flags	5	9
Multiplication / division	No instruction	MUL, DIV, IMUL, IDIV

5. Peripheral Interfacing Chips

Chip	Name	Key features
8255	Programmable Peripheral Interface	3 ports (A, B, C), 24 I/O lines; modes 0 (simple I/O), 1 (handshake), 2 (bidirectional, port A only); BSR mode for port C bits
8253 / 8254	Programmable interval timer	3 independent 16-bit counters, 6 modes
8259	Programmable interrupt controller	8 interrupts per chip, up to 64 by cascading 9 chips
8257 / 8237	DMA controller	4 channels, direct memory to I/O transfer
8251	USART	Serial communication, sync and async
8279	Keyboard / display controller	Scans keys, drives displays

- **Memory-mapped I/O**: devices use memory addresses (all memory instructions work). **I/O-mapped I/O**: separate IN/OUT instructions, 8-bit port address in 8085 (256 ports).
- **Memory interfacing**: number of address lines for the chip = log2(locations). Rest of the lines go to the decoder (chip select).

EXAMPLE A 4 KB memory chip needs 12 address lines (2^12 = 4096). With 16 address lines, 4 lines are left for decoding.

6. 8051 Microcontroller

- 8-bit CPU, 4 KB on-chip ROM, 128 bytes RAM, 4 I/O ports (P0–P3, 32 lines), 2 timers (16-bit), 1 full-duplex serial port, 5 interrupt sources.
- 16-bit address bus (64 KB external program + 64 KB external data memory). 40 pins.
- One machine cycle = 12 clock periods. With 12 MHz crystal, 1 machine cycle = 1 µs.

➤ Internal RAM (128 bytes)

Address	Use
00H–1FH	4 register banks (R0–R7 each), chosen by RS1, RS0 in PSW
20H–2FH	Bit-addressable area (128 bits)
30H–7FH	General purpose (scratch pad), stack
80H–FFH	SFRs (A, B, PSW, SP, DPTR, P0–P3, TMOD, TCON, SCON, IE, IP …)

- On reset: SP = 07H (stack starts at 08H), PC = 0000H, ports = FFH.
- Port 0 needs external pull-up resistors and also works as multiplexed AD0–AD7. Port 2 gives A8–A15. Port 3 has special functions (RxD, TxD, INT0, INT1, T0, T1, WR, RD).

➤ Interrupts of 8051

Source	Vector	Default priority
External INT0	0003H	1 (highest)
Timer 0 (TF0)	000BH	2
External INT1	0013H	3
Timer 1 (TF1)	001BH	4
Serial (RI / TI)	0023H	5

➤ Timers (TMOD register)

Mode	Description
0	13-bit timer
1	16-bit timer
2	8-bit auto-reload (TH loads into TL)
3	Split mode (timer 0 becomes two 8-bit timers)

➤ Solved example (timer delay)

- Generate 1 ms with timer 0, mode 1, crystal 12 MHz.
  - Machine cycle = 12 / 12 MHz = 1 µs, so count needed = 1000
  - Initial value = 65536 − 1000 = 64536 = FC18H
  - Load TH0 = FCH, TL0 = 18H, set TR0 = 1, wait for TF0 = 1

➤ Serial baud rate

FORMULA Mode 1 baud = (2^SMOD / 32) x (fosc / 12) / (256 − TH1), timer 1 in mode 2.

EXAMPLE fosc = 11.0592 MHz, SMOD = 0, TH1 = FDH (253): 11.0592 MHz / 12 = 921600; / 32 = 28800; / 3 = 9600 baud.

➤ Sample 8051 program (toggle P1.0)

```
ORG 0000H
BACK: CPL P1.0       ; complement bit
      ACALL DELAY
      SJMP BACK
DELAY: MOV R2, #250
HERE:  DJNZ R2, HERE ; 2 cycles x 250 = 500 µs at 12 MHz
      RET
```

7. Most Asked Questions (practice)

1. Draw the architecture of 8085 and explain each block.
2. Explain the interrupts of 8085 with vector addresses and priority.
3. Draw the timing diagram of MVI A, 32H and LDA 2050H.
4. Write an 8085 program to find the largest number in an array.
5. Calculate the delay of a given 8085 loop.
6. Explain BIU and EU of 8086. Find the physical address for given CS and IP.
7. Explain the modes of 8255 and write its control word.
8. Explain the internal RAM organisation and SFRs of 8051.
9. Find TH and TL values for a given delay using 8051 timers.
10. Calculate TH1 for a given baud rate in 8051.

TIP In GATE EC, microprocessor questions are few but easy: flags after an operation, T-states, delay counts and memory address decoding. In university exams, practise architecture diagrams and short programs.