VLSI Design

Short notes for B.Tech ECE · M.Tech VLSI · GATE EC

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I. Introduction

- **VLSI** (Very Large Scale Integration) = putting a very large number of transistors on one chip.
- Integration levels: SSI → MSI → LSI → VLSI → ULSI (more transistors at each step).
- **Moore's law** (an observation): transistor count per chip roughly doubles about every two years.
- CMOS is the main technology because static power is almost zero and noise margins are good.

➤ Design styles

Style	Idea	Good	Bad
Full custom	Every transistor drawn by hand	Best speed, area, power	Long design time, costly
Standard cell	Pre-designed cells placed by tools	Good balance, most ASICs	Less optimised than full custom
Gate array	Pre-made transistors, only metal layers custom	Faster to make	Wasted area
FPGA	Programmable logic blocks + routing	No fabrication, reprogrammable	Slower, more power per function

➤ VLSI design flow

```
Specification -> Architecture -> RTL (Verilog/VHDL)
  -> Functional simulation -> Logic synthesis (gate netlist)
  -> Floorplan -> Placement -> Clock tree -> Routing
  -> Timing (STA), DRC, LVS checks -> GDSII (tape-out)
```

- **Y-chart** (Gajski): three views of a design: behavioural, structural, physical.

2. MOS Transistor Review

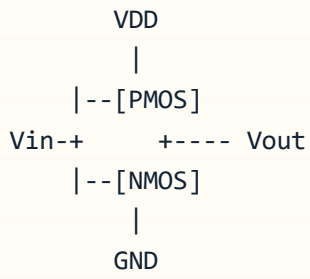
- NMOS: electrons, faster. PMOS: holes, slower (μn ≈ 2 to 3 times μp). So PMOS is made wider for equal current.

> **FORMULA** Saturation: ID = (1/2) μ Cox (W/L) (VGS − VT)^2. Linear: ID = μ Cox (W/L) [(VGS − VT) VDS − VDS^2 / 2].

- **Body effect**: VT = VT0 + γ (sqrt(2ϕF + VSB) − sqrt(2ϕF)).
- **Channel length modulation**: ID rises a little with VDS, factor (1 + λ VDS).
- **Short-channel effects**: velocity saturation, DIBL (drain lowers the barrier, VT falls), hot-carrier effect, punch-through.
- **Leakage**: subthreshold current, gate tunnelling (thin oxide), junction leakage.

3. CMOS Inverter

- PMOS from VDD to output, NMOS from output to ground, gates tied together.
- Input 0 → PMOS ON, NMOS OFF → output = VDD. Input 1 → NMOS ON → output = 0.



➤ Voltage transfer characteristic (VTC) regions

Region	Vin	NMOS	PMOS
A	0 to VTn	Off	Linear
B	Just above VTn	Saturation	Linear
C	VM (switching point)	Saturation	Saturation
D	Above VM	Linear	Saturation
E	Above VDD − abs(VTp)	Linear	Off

> **FORMULA** Noise margins: NMH = VOH − VIH, NML = VIL − VOL. VIL and VIH are where slope of VTC = −1.

EXAMPLE VOH = 1.8 V, VOL = 0 V, VIH = 1.1 V, VIL = 0.7 V. NMH = 1.8 − 1.1 = 0.7 V, NML = 0.7 − 0 = 0.7 V.

- Switching threshold VM = VDD / 2 when βn = βp (symmetric inverter). β = μ Cox W / L.
- Making the PMOS stronger (wider) moves VM up; making the NMOS stronger moves VM down.

➤ Propagation delay

- tpHL (output falls, NMOS discharges CL), tpLH (output rises, PMOS charges CL). tp = (tpHL + tpLH) / 2.
- tp is roughly proportional to CL VDD / I (drive current). Reduce delay: bigger W, smaller CL, higher VDD.
- **Rise time / fall time**: 10% to 90% (or 90% to 10%) of the swing.

4. Power Dissipation

Type	Cause	Formula / note
Dynamic (switching)	Charging and discharging load capacitance	P = α CL VDD^2 f
Short-circuit	Both transistors ON during input transition	Depends on rise/fall times
Static (leakage)	Subthreshold and junction leakage	P = Ileak VDD

FORMULA Dynamic power P = α C VDD^2 f, α = activity factor (fraction of clock cycles with a 0→1 output change).

➤ Solved example (dynamic power)

- C = 10 pF (switched), VDD = 1.2 V, f = 500 MHz, α = 0.2.
  - P = 0.2 x 10 x 10^-12 x (1.2)^2 x 500 x 10^6
  - = 0.2 x 10^-11 x 1.44 x 5 x 10^8
  - = 1.44 mW
  - Halving VDD to 0.6 V would cut this power to one quarter (0.36 mW).
- Low-power ideas: lower VDD (biggest effect, square law), clock gating (lower α), power gating (cuts leakage), multi-VT cells.

- **Power-delay product** (PDP) = P x tp = energy per switching event.

5. CMOS Logic Gates

- **Pull-down network (PDN)** of NMOS + **pull-up network (PUN)** of PMOS. PUN is the dual of PDN.
- Series NMOS = AND, parallel NMOS = OR. The output is the complement of the PDN function.

Gate	NMOS (PDN)	PMOS (PUN)	Transistors
Inverter	1	1	2
2-input NAND	2 in series	2 in parallel	4
2-input NOR	2 in parallel	2 in series	4

- NAND is preferred over NOR: NOR has series PMOS, which is slow (low hole mobility).
- **Complex gate** example: Y = NOT(A·B + C) → PDN: (A series B) in parallel with C. PUN: (A parallel B) in series with C.

➤ Other logic styles

Style	Idea	Note
Pseudo-NMOS	One always-ON PMOS load	Fewer transistors, static power
Pass transistor	Signal passes through a MOS switch	NMOS passes strong 0, weak 1 (VDD − VT)
Transmission gate	NMOS + PMOS in parallel	Passes both 0 and 1 fully
Dynamic (precharge-evaluate)	Clock precharges output, PDN evaluates	Fast, fewer transistors, charge sharing issues
Domino	Dynamic stage + static inverter	Can cascade, but only non-inverting logic

REMEMBER NMOS passes a good 0, PMOS passes a good 1. That is why a transmission gate uses both.

6. Sequential Circuits and Timing

- **Latch**: level sensitive. **Flip-flop**: edge triggered (often two latches in master–slave form).
- **Setup time**: data must be stable before the clock edge. **Hold time**: data must stay stable after the edge.
- **Clock skew**: clock reaches different flip-flops at different times.

> **FORMULA** Setup condition: Tclk >= tclk-q + tlogic(max) + tsetup (+ skew effects). Hold condition: tclk-q + tlogic(min) >= thold.

➤ Solved example (maximum clock frequency)

- tclk-q = 100 ps, longest logic delay = 600 ps, tsetup = 50 ps, no skew.
  - Tclk(min) = 100 + 600 + 50 = 750 ps
  - fmax = 1 / 750 ps = 1.33 GHz
  - Pipelining the logic into two 300 ps stages: Tclk = 100 + 300 + 50 = 450 ps, fmax ≈ 2.22 GHz.

7. Fabrication, Layout and Design Rules

➤ CMOS n-well process (main steps)

1. Start with a p-type wafer; grow oxide.
2. Form the **n-well** (for PMOS) by implantation and drive-in.
3. Define active areas; grow **field oxide** (LOCOS or shallow trench isolation) between devices.
4. Grow thin **gate oxide**; deposit and pattern **polysilicon** gate.
5. **n+ implant** (NMOS source/drain) and **p+ implant** (PMOS source/drain), self-aligned to the gate.
6. Deposit insulator, open **contacts**, deposit and pattern **metal** layers.
7. Add passivation layer.

- **Latch-up**: parasitic p-n-p-n (SCR) path between VDD and GND turns on and shorts the supply. Prevent with guard rings, well/substrate contacts, trench isolation.

Stick diagrams and lambda rules

- **Stick diagram**: colour-coded lines for layers (diffusion, poly, metal), shows topology without sizes.
- **λ-based rules** (Mead–Conway): all sizes are multiples of λ (λ ≈ half the minimum feature). Typical: min poly width = 2λ, poly–poly spacing = 2λ, poly extends 2λ beyond diffusion (exact values depend on the rule set).
- A transistor forms where poly crosses diffusion.
- Checks: **DRC** (design rule check), **LVS** (layout vs schematic), **ERC**, parasitic extraction.

Scaling

Parameter	Constant field scaling (factor S)	Constant voltage scaling
Dimensions (L, W, tox)	1/S	1/S
Supply voltage	1/S	1
Doping	S	S^2
Gate delay	1/S	1/S^2
Power per device	1/S^2	S
Power density	1 (constant)	S^3
Area per device	1/S^2	1/S^2

8. Memories, Testing and HDL

Semiconductor memories

Memory	Cell	Note
SRAM	6T (two cross-coupled inverters + 2 access transistors)	Fast, no refresh, used for cache
DRAM	1TIC (one transistor + capacitor)	Dense, needs refresh, destructive read
Flash	Floating-gate transistor	Non-volatile, block erase
ROM	Fixed connections (mask)	Non-volatile, read only

Testing

- **Stuck-at fault model**: a line stuck at 0 (s-a-0) or stuck at 1 (s-a-1). A circuit with n lines has 2n single stuck-at faults.

- **Controllability** (set a node) and **observability** (see a node at outputs).
- **DFT** (design for testability): scan chains (flip-flops linked into a shift register), BIST (built-in self-test), JTAG boundary scan.

➤ Verilog basics

```
module mux2 (input a, b, sel, output y);
  assign y = sel ? b : a;   // dataflow style
endmodule

always @(posedge clk) q <= d;   // D flip-flop
```

- Use `<=` (non-blocking) in clocked blocks and `=` (blocking) in combinational blocks.
- Modelling styles: gate level, dataflow, behavioural.

9. Most Asked Questions (practice)

1. Explain the VLSI design flow from specification to GDSII.
2. Draw the CMOS inverter VTC and mark all regions; define noise margins.
3. Derive the switching threshold VM of a CMOS inverter.
4. Explain dynamic, short-circuit and leakage power; solve a power numerical.
5. Draw CMOS circuits for NAND, NOR and Y = NOT(AB + CD).
6. Compare static CMOS, pseudo-NMOS, pass transistor and domino logic.
7. Define setup and hold time; find maximum clock frequency.
8. Explain the n-well CMOS process and latch-up.
9. Draw a stick diagram of a CMOS inverter and state λ rules.
10. Compare constant field and constant voltage scaling.

TIP GATE EC asks CMOS inverter, power, logic gate transistor count and setup/hold timing. Draw the PDN first, then make the PUN as its dual.